

539,334

Rec'd PCT/PTO 15 JUN 2005

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

10/539334

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
22 July 2004 (22.07.2004)

PCT

(10) International Publication Number
WO 2004/061724 A1

(51) International Patent Classification⁷: G06F 17/50

05446 (US). MENARD, Daniel, R. [US/US]; 9 Acton Street, Arlington, MA 02476 (US).

(21) International Application Number:
PCT/US2002/040428

(74) Agent: NEFF, Daryl, K.; International Business Machines Corporation, Dept. 18G/Bldg. 300-482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

(22) International Filing Date:
17 December 2002 (17.12.2002)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (for all designated States except US): INTERNATIONAL BUSINESS MACHINES CORPORATION [US/US]; New Orchard Road, Armonk, NJ 10504 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

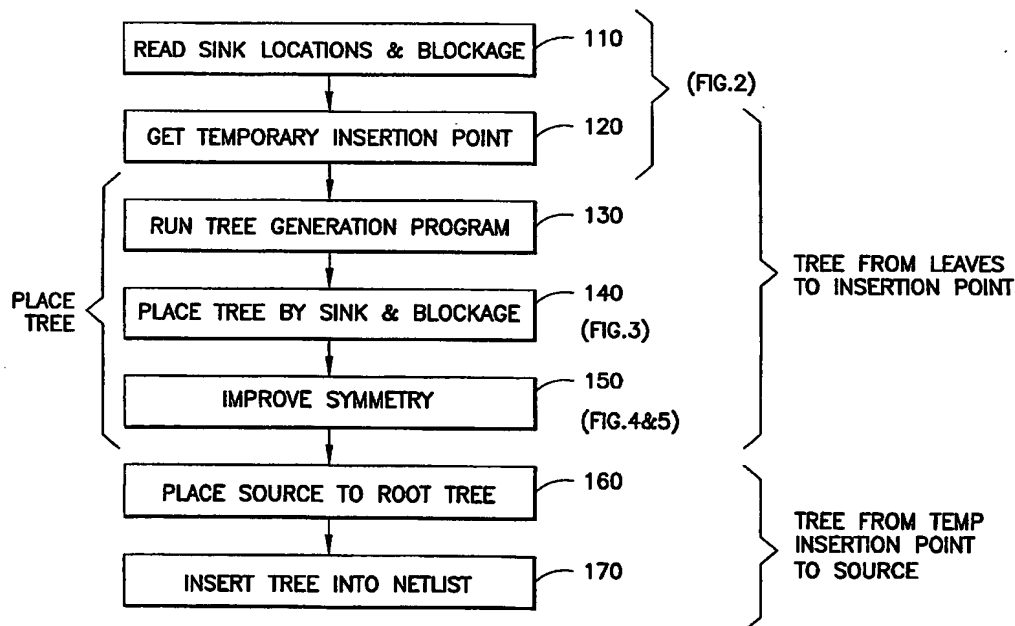
(72) Inventors; and

(75) Inventors/Applicants (for US only): ARTHANARI, Geetha [IN/US]; 38 Thasha Lane, I-4, Essex Junction, VT 05452 (US). CARRIG, Keith, M. [US/US]; 74 South Street, Unit E, Essex Junction, VT 05452 (US). LASHER, Mark, R. [US/US]; 146 Lindale Drive, Colchester, VT

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: ASIC CLOCK FLOOR PLANNING METHOD AND STRUCTURE



(57) Abstract: A method of designing a clock tree in an integrated circuit combines steps of making a list of all clock sinks (110); positioning a temporary reference insertion point (TIP) (120); grouping the sinks together with structured clock buffers (SCBs) in a set of levels (140); and moving the SCBs to improve symmetry of the tree (150). The SCBs may be of several sizes and may be positioned horizontally (42) or vertically (45) and moved within limits (46) to permit the program to calculate a complete tree.

WO 2004/061724 A1